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Keynote Address

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EMC ASPECTS OF FUTURE
HIGH SPEED DIGITAL DESIGNS

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ELECTROMAGNETIC COMPATABILITY
DRIVING FORCES

- Regulations
- Technology
- Signal Integrity
- Time to Market
DIFFERENTIAL - MODE RADIATION

Radiated Emission

PCB

Signal

Ground

\[ E = K_1 f^2 A I_0 \]
CONTROLLING DIFFERENTIAL-MODE EMISSIONS

- Reduce Loop Area
  - PCB Technology Has Not Keep Up With the Increase in Frequency Squared

- Cancellation Techniques
  - Canceling Clock Loops
  - Multiple Decoupling Capacitors

- Spread Spectrum Techniques
  - Clock Dithering
CANCELLATION TECHNIQUES

Clockwise Loop

Counter-Clockwise Loop

SPECTRUM OF A DITHERED CLOCK
(THIRD HARMONIC OF 60 MHz CLOCK)

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COMMON-MODE RADIATION

\[ E = K_2 f L I_{cm} \]

- I/O Cable
- PWB
- Gnd Wire
- Gnd Plane Or Grid
- VN
- Cable
- Equivalent Circuit
- VN
SKIN EFFECT

- Due to the Skin Effect, High Frequency Currents Can Only Penetrate a Metal a Very Small Distance

- Therefore, at High Frequencies all Currents are on the Surface of Conductors, and Cannot Penetrate them.
GROUND RETURN CURRENTS

- Return Currents Will Always Flow on the Nearest Plane
- The Top and Bottom Surfaces of a Plane Act as Separate Conductors
- If The Top and Bottom Surfaces of a Plane Are Used for the Return Current,
  — How Does the Return Current Get From the Top to the Bottom of the Plane?
- If a Mixture of Power and Ground Planes are Used for the Return Current,
  — How Does the Return Current Get From One Plane to the Other?
GROUND CURRENT FLOW

Signal Traces Adjacent to the Same Plane

OK

Signal Traces Adjacent to Different Planes

A Problem Unless We Do Something

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HIGH SPEED CLOCK ROUTING GUIDELINES
(in order of preference)

- Route Clock on One Layer Adjacent to a Plane
- Route Clock on Two Layers, Adjacent to the Same Plane
- Route Clock on Two Layers, Adjacent to Two Planes of the Same Type (i.e., Ground or Power) and Connect Planes Together With a Via Wherever there is a Signal Via
- Route Clock on Two Layers, Adjacent to Two Different Types of Planes (i.e., Ground and Power) and Connect Planes Together With a Decoupling Capacitor Wherever There is a Signal Via
SLOT INDUCED GROUND PLANE VOLTAGE DROP
(3 nS RISE-TIME SQUARE WAVE)

Notes:
- Slot is 0.025” Wide.
- Signal Trace Width is 0.050”.
- Holes = A Pattern of Fifteen 0.052” Diam.
  Holes Along a 1” Line

<table>
<thead>
<tr>
<th>L</th>
<th>V_{AB}</th>
<th>dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 in</td>
<td>15 mV</td>
<td>—</td>
</tr>
<tr>
<td>¼ in</td>
<td>20 mV</td>
<td>2.5</td>
</tr>
<tr>
<td>½ in</td>
<td>26 mV</td>
<td>4.8</td>
</tr>
<tr>
<td>1 in</td>
<td>49 mV</td>
<td>10.3</td>
</tr>
<tr>
<td>1½ in</td>
<td>75 mV</td>
<td>14.0</td>
</tr>
<tr>
<td>Holes</td>
<td>15+ mV</td>
<td>—</td>
</tr>
</tbody>
</table>
We Must Learn To Ask The Question,

Where Does The Return Current Flow?
Ground Plane Current Distribution

- Trace on Opposite Side of Board
- Constriction of Current, High Inductance
- Current Spreads Out, Low Inductance
- Constriction of Current, High Inductance
- Via
Ground Plane Voltage Measurements
(Peak to Peak Voltage)

6"

Ground Plane

15 mV 15 mV 15 mV 88 mV

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HOC
ELECTROMAGNETIC COMPATIBILITY
GROUND PLANE INDUCTANCE NEAR VIA

nH/inch

Inches from Via

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ELECTROMAGNETIC COMPATIBILITY
DECOUPLING NETWORK - EQUIVALENT CIRCUIT

Decoupling Capacitor

PWB Trace Inductance

Integrated Circuit

2\eta H

R

C

R

3\eta H

5\eta H

15\eta H

5\eta H

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HOC
ELECTROMAGNETIC COMPATIBILITY
MUTIPLE CAPACITORS

General Equation

\[ \begin{align*}
C_t &= NC \\
L_t &= L/N
\end{align*} \]

For \( N \) Capacitors of Value \( C \), Each in Series With an Inductance \( L \)
DECOUPLING

- It is Difficult to Achieve Good Decoupling at High Frequencies (> 50 MHz)
- One Way to Achieve This is With Multiple Capacitors (2-50)
  - Make Them The Same Value
  - Spread Them Out Physically
- Another Approach is by Using Embedded PCB Capacitance
- Interdigitated Power & Ground Pins Helps Lower the IC Lead Inductance
- One of the Biggest Limitations in Using Decoupling Capacitors is the Inductance of the Pad to Via Trace.
  - Use Multiple Vias, or
  - Pad in Via Technology to Reduce This
- Another Approach is to use Multiple Capacitors Inside the IC Package Itself
- Isolated Power Planes Can be Helpful in Minimizing the Bad Side Effect of Poor Decoupling But Does Not Solve the Basic Problem
SIGNAL INTEGRITY (SI) & EMC

- Signal Integrity: How a Signal Effects Itself
- Signal Integrity: Usually Concerned With Millivolts & Milliamps
- EMC: How a Signal Effects Others
- EMC: Usually Concerned With Microvolts & Microamps
EMC & SIGNAL INTEGRITY

EMC & Signal Integrity

Electrical Design

Physical PCB Layout
ELECTRICAL & PHYSICAL PARAMETERS

- Physical PCB Layout
  - Copper
  - Dielectric
  - Traces
  - Vias
  - Pads

- Electrical Parameters
  - Inductance
  - Capacitance
  - Resistance
  - Characteristic Impedance

- This is What We Build

- This is What The Signal Sees
THERE ARE FOUR SOURCES OF SIGNAL DISTORTION

- The Signal Net Itself
  - Discontinuities
  - Reflections
  - Attenuation
- Crosstalk
- Power & Ground Noise
  - Ground Bounce
  - Decoupling
- External Noise Sources
  - Radiated
  - Conducted
HIGH DENSITY INTERCONNECT

- Chip Scale Packaging (CSP)
  - Ball Grid Arrays
  - Chip on Board
  - Flip Chip
  - Reduced Pkg. Inductance
- System on a Chip (SOC)
  - Large I/O Counts (>500)
- PCB Layout/Stackup
  - Closer Spaced Layers
  - Elimination of Surface Layer Traces
  - Transmission Lines
  - Faraday Shields
- Testability Issues
  - Test Point Access
- PCB Materials
  - FR-4
  - Polyamide
  - Ceramic/Glass
  - PolyTetraFluroEthelyne (PTFE)
- Vias
  - Microvias (<6 mil)
  - Via in Pad
  - Blind Vias
  - Buried Vias
- Drilling Techniques
  - Laser
  - Plasma
  - Photo-Defined

Denser, Faster, Smaller
IC PACKAGE INDUCTANCE

Ref: Lau, p. 37
TRANSMISSION LINE LOSSES

- Skin Effect
- Dielectric Loss
- Ground Plane Loss
- Surface Roughness
- Radiation Losses
SUMMARY
(TRANSMISSION LINE LOSSES)

- For Traces Shorter Than 12” You Can Usually Ignore all Losses up to 1 GHz.
- Above 1 GHz Skin Effect Losses Become Significant
- Above 3 GHz Dielectric Losses Become Predominant
IN SUMMARY

- The Difference Between Signal Integrity (SI) & EMC is *Why* You Do Something, Not *What* You Do

  - For EMC You Do Something to Minimize the Emissions and Susceptibility or For Regulatory Compliance

  - For Signal Integrity You Do The Same Thing to Make the Circuit Work Reliably
NEW TECHNOLOGY

- Evolution of New Technology
  - State of the Art
  - Leading Edge
  - Commodity
- Embedded Capacitance
- Micro-Vias, Buried Vias. Blind Vias
- Chip Scale Packaging
- New PCB Materials
BE INNOVATIVE

- Understand the Basic Principles of EMC & SI and Apply them in New Innovative Ways
- Don’t be Afraid to Do Things Differently
- Fund Some R & D With Respect to EMC & SI
- Consider New Technologies
- What’s New Today Will Probably be Common Tomorrow
- Continue to Learn and Educate Yourself
- Remember, Whatever You Did Last Time Will Probably Not Work Next Time
REFERENCES